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Enhancing FD-SOI MOSFET Performance and Reliability: A Comparative Study of High-k TiO_2 versus Standard SiO_2 Buried Oxides

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Abstract

The continuous downscaling of CMOS technology forces us to use material integration. Novel material integration helps us get past the limits of standard Silicon-On-Insulator (SOI) architectures. In this paper we study the performance and reliability of Depleted SOI (FD-SOI) MOSFETs when we replace the conventional Silicon Dioxide (SiO_2) Buried Oxide (BOX) with a high-permittivity Rutile-phase Titanium Dioxide (TiO_2, $\varepsilon \approx 80$). We focus on Depleted SOI (FD-SOI) MOSFETs. Through analysis and Silvaco TCAD simulations we show that the high-k BOX significantly enhances vertical capacitive coupling. The high-k BOX increases the saturation drain I_{ON} from 1.75 mA to over 2.8 mA compared with the standard reference. The high-k BOX does not cause a threshold voltage shift. The high permittivity lets the dielectric layer be physically thicker while the equivalent capacitance stays the same. The high permittivity also suppresses the tunneling leakage currents dramatically. The high permittivity reduces the reliability issues such as Time-Dependent Dielectric Breakdown TDDB. Beyond electrical characterization, this study evaluates the industrial feasibility of the proposed architecture. We analyze critical manufacturing challenges, including Atomic Layer Deposition (ALD) throughput, wafer bonding defects, and thermal instability due to crystallization. Finally, a comparative economic analysis reveals that the modified TiO_2 SOI process entails production

costs exceeding five times that of standard Bulk MOSFETs, currently restricting this technology to ultra-high-performance niche applications in aerospace and military sectors.

Keywords

FD-SOI, High-k Dielectrics, Titanium Dioxide (TiO_2), Buried Oxide (BOX), TCAD Simulation, MOSFET Reliability, Wafer Bonding, Manufacturing Cost Analysis.

1. Introduction

The constant change in microelectronics asks for transistor miniaturisation. That pushes MOSFETs toward their physical and cost limits. We see that the performance and reliability needed for technology nodes are high. The silicon-on-insulator (Fully *Depleted* -SOI) architecture appears as a good alternative. The silicon-on-insulator (FD-SOI) architecture gives better isolation and better control of the electric field. Although the performance of the fully-depleted silicon-on-insulator devices still depends on the properties of the buried oxide (BOX).

The buried oxide (BOX) is usually made of silicon dioxide (SiO_2), the dielectric constant of this standard material makes it hard to improve capacitive coupling, it also forces the physical thickness to stay thin, that we know has to stay thin to keep reliability against ageing effects such, as bias-temperature instability (BTI) and dielectric breakdown.

This paper presents an in-depth comparative study investigating the replacement of the standard BOX with a high-k material, specifically rutile-phase titanium dioxide (TiO_2). Combining theoretical analysis of reliability parameters with Silvaco TCAD simulations, we demonstrate how increasing the dielectric constant influences drain current (I_{ON}) and device robustness. Moreover, the study goes beyond purely electrical considerations to assess the industrial feasibility of this architecture, confronting manufacturing challenges—particularly deposition and thermal stability—with the economic realities of production costs relative to conventional bulk and SOI technologies.

2. Permittivity and MOSFET Reliability

In a MOSFET permittivity ε controls the field and the capacitance. A higher permittivity lets the electric field stress relax while the performance stays the same. The higher permittivity then helps the device live longer.

2.1. *Reduction of Threshold Voltage Shift (ΔV_{th})*

Reduction of Threshold Voltage Shift **(V_{th})** is the reason for reliability (especially, for fighting BTI effects. Bias Temperature Instability). As a transistor ages, parasitic charges Q_{it} (or trapped charges) accumulate at the interface or within the oxide. The formula for the threshold voltage shift is:

$$\Delta V_{th} = -\frac{\Delta Q_{it}}{C_{ox}}$$

However, the surface oxide capacitance C_{ox} depends directly on the permittivity of the oxide insulator ε_{ox} and its physical thickness t_{ox}:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

By combining the two, we obtain:

$$\Delta V_{th} = -\frac{\Delta Q_{it} \,.\, t_{ox}}{\varepsilon_{ox}}$$

For the same amount of trapped charges (Q_{it}), if the oxide permittivity (ε_{ox}) is higher (as it is for TiO_2), the threshold voltage shift (ΔV_{th}) is lower. The transistor remains stable for longer: it is therefore more reliable.[2]

2.2. *Electric Field in the Oxide and Breakdown (TDDB)*

The reliability of the insulator (Time-Dependent Dielectric Breakdown) depends exponentially on the field. The electric field passes through the insulator.

Gausss law says that at the silicon/insulator interface the electric displacement vector (D) stays the same. The silicon/insulator interface does not change the displacement vector (D).

$$D = \varepsilon_{Si} E_{Si} = \varepsilon_{ox} E_{ox}$$

The result gives the field in the oxide:

$$E_{ox} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} E_{Si}$$

Reliability Interpretation:

We notice that if we increase ε_{ox} ,the field in the channel E_{Si} stays the same. We can also see that the electric field that stresses the oxide E_{ox} then decreases. The oxide E_{ox} field goes down as ε_{ox} goes up.

Less field = less stress = increased lifetime before breakdown.

2.3. Tunneling Current (Grid Leakage and Heating)

To ensure long-term device reliability and mitigate self-heating effects, it is imperative to limit gate leakage current. This leakage, often governed by Fowler-Nordheim tunneling, is critically dependent on the physical thickness of the dielectric barrier. In order to maintain the same electrostatic control capacity (C_{ox}) as a standard silicon dioxide layer while integrating alternative materials, the concept of Equivalent Oxide Thickness (EOT) is employed. This relationship is defined as:

$$EOT = t_{high-k} \left(\frac{\varepsilon_{SiO2}}{\varepsilon_{high-k}} \right)$$

where t_{high-k} represents the physical thickness of the high-permittivity layer. By utilizing a high-k material, the physical thickness t_{phys}can be increased while keeping the EOT constant. Since the tunneling current (J) is approximately proportional to $\alpha\ exp(-\alpha\ .\ t_{phys})$ This increased physical thickness exponentially suppresses electron tunneling, thereby reducing heat generation and the risk of premature dielectric breakdown.

Reliability Interpretation:

By increasing high-k, we can increase the physical thickness t_{phys}while maintaining the same electrical performance (constant EOT).

A thicker layer blocks electrons exponentially better, reducing heating and the risk of premature breakdown.[3]

2.4. Characteristic Length (Control of Short Channel Effects)

In our design we define a length (λ) to keep the structure reliable and to stop the drain from taking too much control over the gate. The Drain-Induced Barrier Lowering (DIBL) effect describes the situation where the drain pulls the gate down. A smaller characteristic length λ shows that the component is more robust. Engineers approximate the length (λ) for a MOSFET, with the following equation:

$$\lambda = \sqrt{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{si}.t_{ox}}$$

Reliability Interpretation:

We have found that higher oxide permittivity (ε_{ox}) makes the characteristic length λ smaller. The smaller characteristic length helps the gate lock onto the channel tightly. The tighter electrostatic locking of the gate onto the channel makes the device more reliable when the drain voltage (V_{DS}) changes.

3. Simulation

Titanium dioxide (TiO_2) is a solid that stays stable when heated. We notice that Titanium dioxide (TiO_2) is very white blocks the light and stops the UV so Titanium dioxide (TiO_2) works as a sun blocker and as a catalyst that works with light to break down the pollutants. Titanium dioxide (TiO_2) has properties that let Titanium dioxide (TiO_2) work with electricity. We see that Titanium dioxide (TiO_2) is chemically stable and not toxic when Titanium dioxide (TiO_2) is in the form. We also see that Titanium dioxide (TiO_2) comes in crystal forms called rutile and anatase and those forms are important, for the paints,

the plastics, the cosmetics and the environmental engineering. We have used Titanium dioxide (TiO_2) in projects.

3.1. Permittivity ($\varepsilon_r \approx 80$)

When we look at the material we notice the flagship property is the dielectric constant. TiO_2 in the Rutile phase shows a very high dielectric constant. TiO_2 dielectric constant exceeds the constant of standard SiO_2 which is 3.9 or the dielectric constant of HfO_2 which is about 25.

Advantage: The Buried Oxide (BOX) creates electrostatic coupling. The Id-Vd curves show the coupling. The Buried Oxide (BOX) also lets the device have a physical thickness while the device keeps a high equivalent capacitance (EOT).

3.2. Band Gap and Band Offset (The Critical Trade-off)

We notice the compromise in reliability. We also notice the compromise in leakage current.

Band Gap (E_g): TiO_2 is a wide-bandgap semiconductor (3.0 eV) rather than a perfect insulator like SiO_2 (9 eV).

Barrier (ΔE_C): The conduction band offset compared to Silicon is very low. Sometimes the conduction band offset is, to 0 eV depending on the interface. Often the conduction band offset is 1.0 eV.

Consequence: The barrier that electrons go through by tunneling is low. The low barrier makes the transmission coefficient higher.

Counter-measure: The material is placed as a layer to cut down the issue. For example the material can sit in a 50 nm BOX. If the material is made into a thin gate insulator (2 nm) the leakage currents rise too high even though the material still has the high-k property.[4]

3.3. Crystalline Phases (Polymorphism)

In applications TiO_2 appears mainly in two forms:

Anatase is a form that's not stable and can stay for a while. Anatase forms crystals at the temperatures $\varepsilon_r \approx 30 - 40$. $E_g \approx 3.2\, eV$.

Rutile is the form that appears after annealing at high temperatures (> 700°C). Rutile gives the permittivity ($\varepsilon_r \approx 80 - 100$ or more depending on crystal orientation).

Note: The simulation assumes the crystallization is in the Rutile phase. The $\varepsilon_r \approx 80$.

These values are standard in semiconductor physics. TiO_2 can appear in crystal forms. The simulation uses the Rutile phase of TiO_2 to get a permittivity of 80.[5]

Table 1: Comparison of Physical and Electrical Properties between Rutile-Phase Titanium Dioxide (TiO_2) and Standard Silicon Dioxide (SiO_2) used in Simulations.

Property	Typical Value du TiO_2 Rutile	Comparison SiO_2 (Standard)
Dielectric Constant	80 - 110	3.9
Band Gap	3.0 - 3.1 eV	~9.0 eV
Electron Affinity	~ 4.0 eV	~ 0.9 eV
Conduction Band Offset	~ 0.0 - 1.0 eV (Faible)	3.1 - 3.5 eV
Refractive Index	2.6 - 2.9	1.46
Density	4.23 g/cm³	2.2 g/cm³
Melting Point	1843 °C	~1700 °C

4. Results

We looked at the figure. The simulated output characteristics ($I_D - V_D$) show a difference in the ON-state current (I_{ON}) between the standard SOI structure and the modified High-k structure. We see the gap clearly. The reference device with a SiO_2 BOX $\varepsilon_r = 3.9$, curve) saturates at about 1.75 mA. The device with a TiO_2 BOX ($\varepsilon_r \approx 80$ curve) reaches a saturation current, above 2.8 mA.

We see that the improvement in drain current is not linked to a shift in the threshold voltage (V_{th}). The curve behavior at drain voltages ($V_{DS} \rightarrow 0$) shows that the devices start to conduct at similar voltages. The observation suggests that the performance gain does not come from a change in the switching point. The performance gain comes from charge transport efficiency in the channel during the ON state.

We see that the phenomenon means the vertical capacitive coupling gets stronger because the buried material has permittivity. We find that in an FD-SOI architecture the channel potential follows a capacitive coupling. The double capacitive coupling comes from the gate (C_{ox}) and from the back gate, through the BOX (C_{BOX}). The BOX capacitance follows the relation:

The use of TiO_2 increases the permittivity $\varepsilon_{BOX}$by a factor of more than 20 compared to SiO_2. This drastic increase in buried capacitance improves the global electrostatic control over the channel. Consequently, for a given gate voltage ($V_{GS} > V_{th}$), the inversion charge density (Q_{inv}) available in the channel is significantly higher in the TiO_2 structure. Since the drain current is proportional to this charge, the modified structure delivers a higher current, reflecting a better effective transconductance of the device.

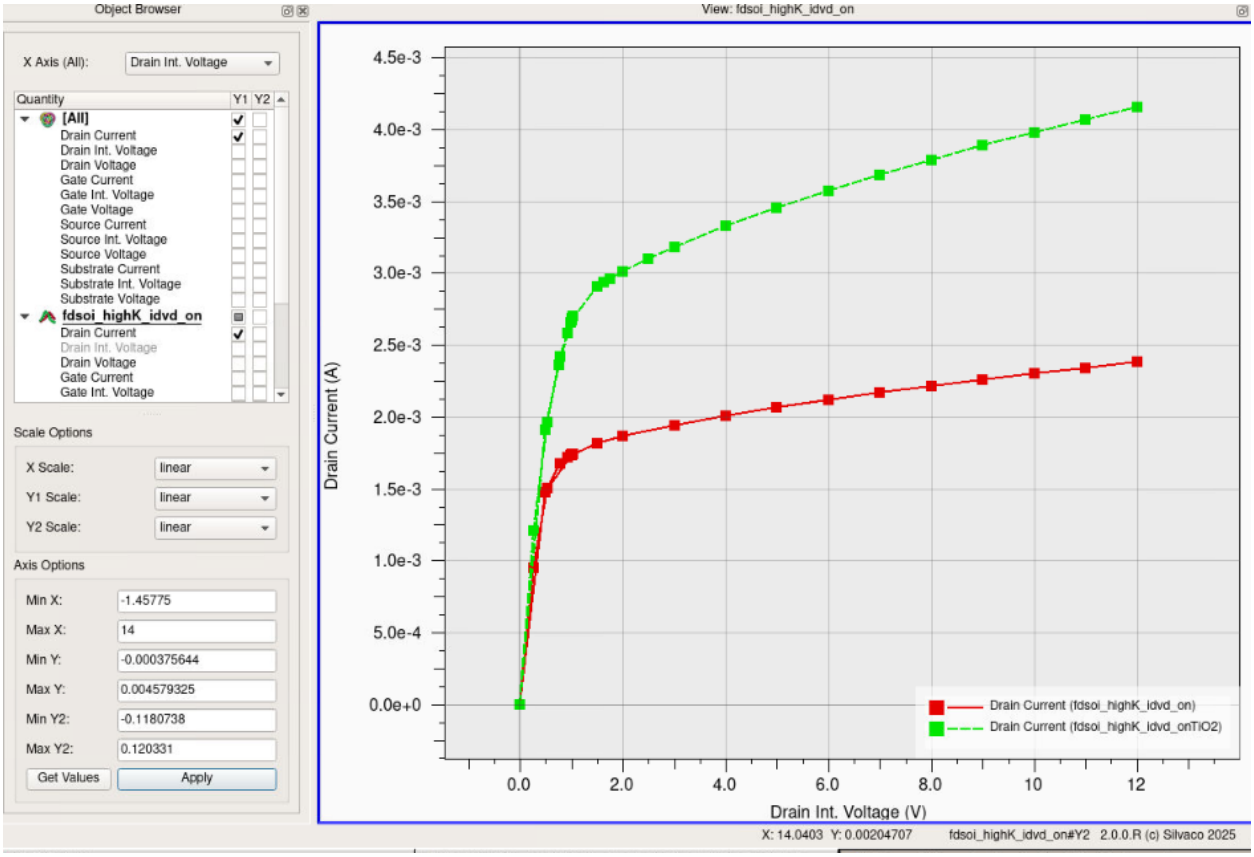

Figure 1: Simulated Output Characteristics ($I_D - V_{DS}$). comparison of the saturation drain current (I_{ON}) between the reference FD-SOI device with a standard SiO_2 BOX (red curve) and the modified architecture integrating a High-k TiO_2BOX (green curve).

We've compared the simulated subthreshold characteristics. We can see a big change in device performance that comes from the buried oxide layer. The change is clear. When I look at the drain current versus gate voltage plot we see that adding a high-permittivity (high-k) material to the BOX structure makes the device switch differently than the standard FDSOI reference. The high-k BOX device shows a drop in threshold voltage. The high-k BOX device turns on at **0.28 V**. The standard FDSOI counterpart needs a gate bias of **0.40 V** to turn on. The standard FDSOI counterpart reaches the conduction state only after the higher gate bias. The lower threshold voltage for the high-k BOX device comes from capacitive coupling between the back-gate and the channel. The k dielectric causes stronger capacitive coupling, between the back-gate and the channel. Consequently, this stronger electrostatic control allows the channel to invert at lower

applied voltages, indicating that the high-k BOX architecture offers potential advantages for applications requiring reduced operating voltages, provided that off-state leakage currents remain manageable.

5. MOSFET Manufacturing Method: The Challenge of the "Exotic" TiO_2 Insulator

The fundamental difference lies in the fact that silicon dioxide (SiO_2) is "native" to silicon (it can be grown by heating the silicon), while titanium dioxide $(TiO_2)$is an "exogenous" material (it must be brought in and deposited).

5.1. The Formation Method

SiO_2 Thermal Oxidation:

We've used Thermal Oxidation as we found it to be the simplest and most pure method. We place the silicon wafer in a temperature furnace (>800°C) with oxygen. Thermal Oxidation grows SiO_2 by consuming the surface silicon.

The SIMOX Process bombards silicon with energetic oxygen ions. Then the SIMOX Process performs an annealing step, then we can see the oxide forms under the surface.

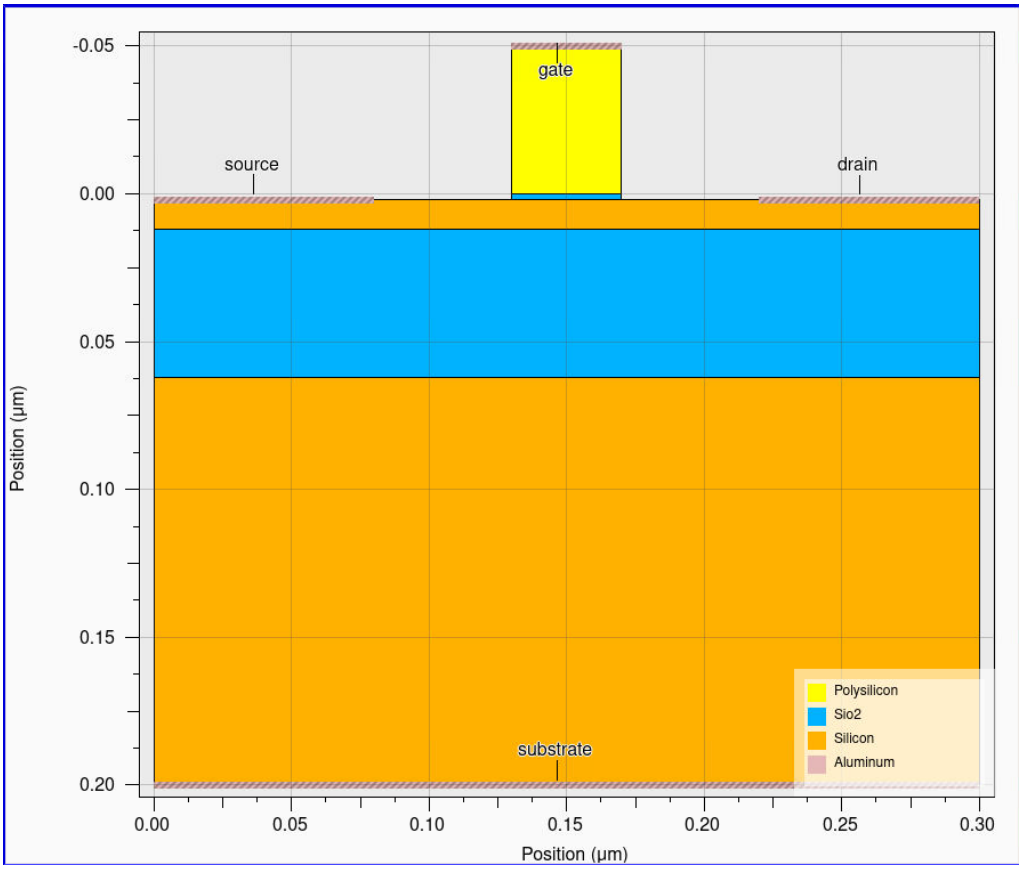

Figure 2: 2D Cross-Sectional View of the Reference FD-SOI MOSFET. The structure features a standard Silicon Dioxide (SiO_2) Buried Oxide (BOX) layer formed via thermal oxidation or SIMOX process by Silvaco TCAD.

5.2. TiO_2 (Modified) Mandatory Deposition

TiO_2cannot grow from silicon. We must deposit TiO_2 using methods such as ALD (Atomic Layer Deposition) for precision or CVD (Chemical Vapor Deposition).

We cannot use the SIMOX process to create a buried oxide layer (BOX), with TiO_2. Instead the Smart-Cut™ technique is required (Wafer Bonding) : we put the TiO_2onto one wafer (the handle or donor wafer). We join the two wafers together. We thin the wafers.[4]

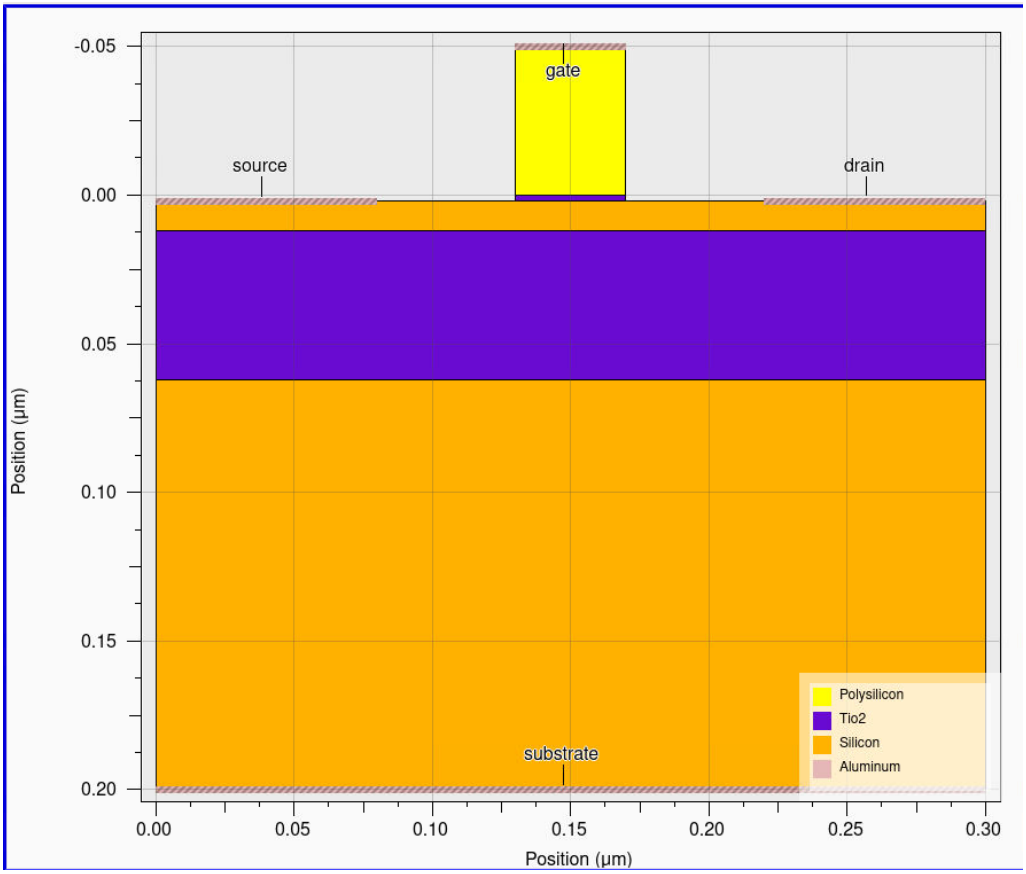

Figure 3: 2D Cross-Sectional View of the Modified High-k FD-SOI MOSFET. The architecture integrates a Rutile-phase Titanium Dioxide (TiO_2) Buried Oxide layer, theoretically integrated via wafer bonding techniques.

5.3. The Thermal Budget and Crystallization

The biggest challenge with TiO_2 is that TiO_2 does not crystallize easily. SiO_2 stays amorphous (no ordered crystal structure) at very high temperatures up to the melting point of silicon. We think this is ideal because an amorphous insulator blocks current. The amorphous insulator does not make grain boundaries that let leak. We deposit TiO_2 at temperatures and it stays amorphous. When we heat TiO_2 (for dopant activation anneals, >600 °C) crystallizes. TiO_2 changes to the Anatase phase first. Then it changes to the Rutile phase, at temperatures.

The problem is that the crystallization creates the grain boundaries, which're possible paths for electrons to leak. The crystallization changes the material volume and creates mechanical stress.

The mechanical stress cracks the wafer. Deforms the silicon channel that sits just above the wafer.

5.4. The Interface Quality (D_{it}– Interface Trap Density)

Si/SiO_2 Interface: The Si/SiO_2 interface has few electronic defects. This interface has a low D_{it}. Oxygen passivates the silicon dangling bonds.

Si / TiO_2 Interface:

We have observed that the Si / TiO_2 interface is thermodynamically unstable. When you place TiO_2 directly against Si and heat the stack, the TiO_2 can form Titanium Silicide ($TiSi$). Can cause an oxidation-reduction reaction in which the titanium steals oxygen. The lattice mismatch between Si and TiO_2 creates interface defects. The defect density D_{it} is high and the high D_{it} reduces the mobility of the carriers, in the channel above.[5]

Often-necessary solution: An ultra-thin 0.5 to 1 nm layer of SiO_2 or $SiON$ is frequently inserted between the Si and the TiO_2 to act as a buffer layer.

The following table summarizes the comparison between standard SiO_2 BOX and modified high-k TiO_2 BOX.

Table 2: Comparative Summary of Fabrication Methods, Material Characteristics, and Integration Challenges for Standard SiO_2 versus Modified High-k TiO_2 Buried Oxide Layers.

Feature	**Standard SiO_2 BOX**	**Modified High-k TiO_2BOX**
Creation Method	Thermal Oxidation or Implantation (SIMOX)	Deposition (ALD, CVD, PVD) + Wafer Bonding

Structure	Amorphous (highly stable)	Polymorphic (Amorphous →Anatase → Rutile with temperature)
Permittivity (ε_r)	~ 3.9 (Low)	~ 80 (Rutile Phase)
Interface Quality (D_{it})	Excellent (very low trap density)	Poor (often requires an interfacial SiO_2 buffer layer)
Thermodynamic Stability	Very High (inert with Si)	Medium (risk of TiSi or silicate formation at the interface)
Main Drawbacks	Low thermal dissipation, weak capacitive coupling 12	Higher leakage currents (low band gap), integration complexity 13

6. Component manufacturing cost

The cost of a semiconductor depends not only on the raw material, but especially on the complexity of the process (number of masks), the yield and the cost of the starting substrate.

In this comparison, we will take as a reference the manufacturing cost of a conventional bulk MOSFET.

6.1. Conventional Bulk MOSFET manufacturing cost

We've seen the industry technology change over four decades. The industry standard technology is still the choice for regular semiconductor making.

Wafer (substrate) cost: **low** – a 300 mm silicon wafer is the raw material you can find. The wafer usually costs about $100 to $150, per wafer.

Process cost: **moderate to high**. Fabricating transistors on silicon is complex. Fabricating transistors on silicon needs the deep N- and P-type wells to electrically isolate each device. Fabricating transistors on silicon also needs the extra lateral-isolation steps such as shallow-trench isolation (STI). Fabricating transistors, on silicon requires the extra lithography masks to reduce latch-up susceptibility.[1]

Despite the high number of processing steps, the massive economies of scale associated with bulk-silicon production make this the globally **least-expensive** solution for CMOS manufacturing.

6.2. Classic SOI (BOX $Si0_2$) manufacturing cost

The mature technology gives performance and low power consumption. STMicroelectronics and GlobalFoundries use this technology while producing their MOSFET.

Wafer (Substrate) Cost: **High**. We've seen that the SOI wafer costs **three to four times more than** the wafer. The cost is a lot higher.

The reason is that the Smart-Cut™ process, from Soitec, needs two silicon wafers to make one wafer. We notice that the two silicon wafers are a donor wafer and a support wafer. This process adds hydrogen implantation and then performs annealing steps.[1]

Process Cost: **Medium/Low.**The advantage of SOI is that the process is simplified. No need to create deep wells. Simpler lateral insulation.

The final cost of the chip is approximately **10-15% higher than bulk**. The increased cost of the substrate is only partially offset by the simplified process. This additional cost is justified by the performance gain (+20%) or the reduction in consumption.[2]

6.3. Modified SOI (BOX high-k TiO_2) manufacturing cost

This is our research structure.

Wafer (Substrate) Cost: **Extremely High** .

There is no mass production. Each wafer must be fabricated "custom-made" in a laboratory or pilot factory. TiO_2 must be deposited (ALD/CVD) on an entire plate, which is slow and expensive, unlike SiO_2 which is native (grown directly).

Process Cost: **Very High**.

Titanium is often considered a contaminant in standard CMOS production lines (cross-contamination risk). Dedicated machines are required which make the integration complex. Depositing a thick layer (50nm) of TiO_2 by ALD (Atomic Layer Deposition) takes a lot of time (several hours) compared to rapid thermal oxidation.

The difficulty of bonding (Wafer Bonding) between Si (silicon) and TiO_2 creates voids or defects.

The mechanical stress due to the crystallization of TiO_2 can break the wafers or render the transistors inoperable.[3]

To summarize, the modified SOI that we propose still has a prohibitive cost for now. It should be reserved for niche applications (aerospace, military, very high sensitivity sensors) where price is not the limiting factor.

The following table summarizes the relative manufacturing costs associated with each technology.

Table 3: Relative Manufacturing Cost and Process Complexity Analysis: Comparison of Conventional Bulk, Standard FD-SOI, and Modified High-k SOI Technologies.

Cost Factor	Conventional Bulk MOSFET	Classic SOI (SiO2)	Modified SOI (TiO2 High-k)
Raw Material (Wafer)	1x (Ref)	3x - 4x	> 20x (Prototype)
Complexity (Masks)	High (Complex isolation)	Medium (Simplified isolation)	High (Decontamination management)
Required Equipment	Standard	Standard	Specific (ALD + Special Bonding)
Yield	> 99%	> 98%	Low (Interface defects)
Estimated Total Cost per Chip	**Index 100**	**Index 115**	**Index > 500**

7. Conclusion

In conclusion the high-permittivity buried oxide made of TiO_2 ($\varepsilon_r \approx 80$) placed in the FD-SOI architecture shows promise for improving the electrical performance and the intrinsic reliability of the transistors. The simulations show that the device can deliver a higher saturation current than the standard SOI. The saturation current rises from 1.75 mA to over 2.8 mA. The increase comes from a vertical capacitive coupling. The threshold voltage does not shift significantly. The high-permittivity buried oxide is the element that makes the improvement possible.

In our view reliability comes from what theory says about the high-k material. Theory says that the high-k material lets the physical layer be thicker while the control capacitance stays the same. The high-k material's layer cuts tunnelling leakage currents a lot. The high-k material's thicker layer also cuts the risk of breakdown which is called Time-Dependent Dielectric Breakdown (TDDB).

However, the transition to this "modified" technology faces considerable industrial and economic barriers. Unlike native SiO_2, TiO_2 requires complex and costly fabrication processes such as atomic-layer deposition (ALD) and wafer bonding, and it presents challenges in thermal stability and interface quality. Economic analysis indicates a prohibitive production cost, estimated at more than five times that of a standard bulk MOSFET, which currently limits this architecture to ultra-high-performance niche applications (aerospace, military) where cost is not the primary constraint.

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